CAD of Integrated Passives on Printed Circuit Boards Through Utilization of Multiple Material Domains

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Abstract — **With the addition of microvia and other organic layer technologies, integrated passives on Printed Circuit Boards (PCB) are a possible way to reduce the cost and size of designs in FR4 and similar panelized manufacturing processes; however, the actual deployment of this design methodology has been limited by CAD tools and current design methodologies. In this paper, a CAD methodology for PCB's is presented that defines correlated component representations in two material stratifications. One is similar to the current SMT component approach whereas the other is an integrated passives approach. By specifying the materials carefully and creating a mapping of components between the two physical domains, a product development methodology is described that combines the best characteristics of both domains while minimizing risk.**

I. INTRODUCTION

The potential for a wide variety of integrated passives on organic Printed Circuit Boards (PCB's) has expanded over the last few years [1][2][3] with the introduction of microvias, composite dielectric materials [4][5][6], and solder ball technologies. Techniques used to model integrated passives for integrated circuits on GaAs, Silicon and other insulating and semi-insulating substrate materials are being used to model structures on organic PCB's [7][8][9]. However, integrated passives incorporated on printed circuit boards using FR4 or other paneled materials have seen limited production numbers. Some of the issues behind the slow incorporation of integrated passives into PCBs relate to time-to-market pressures, a need for rapid prototyping and engineering changes. This methodology addresses these issues.

With PCB's, design issues are most often caused by unwanted signal contamination, coupling between rooms of a board, or circuit performance degradation as a result of component variation (specified or unspecified parameters). As a result, the design methodology for PCB circuits has minimal computer aided design up front and relies on swapping production ready Surface Mount Technology (SMT) components to achieve the desired circuit or system performance. The most productive and skilled RF and Microwave designers using PCB technologies uses a complementary combination of measurements on the bench and simulation to understand details of the circuit performance, anticipate component changes, and produce manufacturable designs.

As a design evolves towards production, specific aspects of the board are frozen. Production teams are tasked with making changes in order to reduce costs; however, in order to reduce risk, redesign is minimal and most components remain frozen in the design (although alternate equivalent SMT parts may be substituted to reduce costs). Layout changes are minimized (including transforming passive components into integrated passive form) to contain risk.

By generating correlated (RLC) components that have representations for the prototype phase (Fig 1a. with SMT benefits) and the production phase (Fig 1b. with integrated passive benefits), the risks associated with the cost reduction phase are reduced resulting in greater efficiency and productivity without a loss in design efficiency.

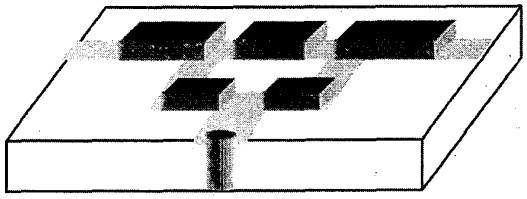

Fig. 1a. Prototype Board with FR4 Core Board with mapped SMT discrete valued components.

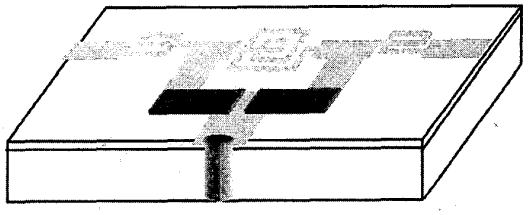

Fig. 1b. Production Board with microvia integrated passives for capacitors and inductors.

In this paper, a general CAD structure is defined that enables efficient CAD automation enabling rapid component realization, and correlation of component models over multiple material specifications. The systematic (scripted) generation of component models

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based on the Electrical Parameters and Technology Files is essential to efficient library generation. The resulting range of realizable component values is presented in a Synthesis Parameter File. A mapping between multiple Synthesis Parameter Files enables component transformations between the two material domains with minimal risk.

II. CAD Structure

A scripted automated procedure is used to generate the RLC component realizations based on the technology and electrical parameters. By defining I/O structures for a Technology, Electrical, and a Synthesis Parameter File these scripts can be reused as the base technology evolves.

A. Technology File

Specific base values and statistics describing the material and processing parameters are defined in the Technology File. This will include substrate material properties (er, tand, ur, thickness), metalization parameters (thickness, conductivity), processing parameters (via sizes on and through each layer, etch factor, layer dependencies, etc.) and any other physical definitions (minimum line width and spacing). These parameters must include tolerances and standard deviations (or ranges and cpk values) to allow generation of the proper electrical statistical behavior based on the statistical behavior of the physical parameters.

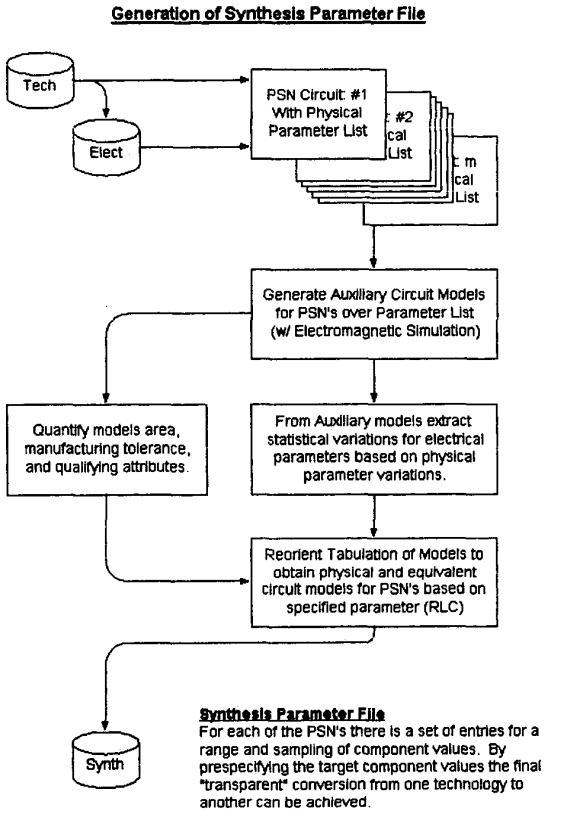
B. Electrical Parameter File

Utilizing data from the technology file, analytical expressions or 2D electromagnetic simulations are used to determine the derived parameters in the Electrical Parameter File. These derived parameters include the synthesized transmission line characteristics (impedance, loss, and er_{eff}) for single and coupled transmission lines on each of the signal layers with the different ground configurations. The tabulated transmission lines include minimum width lines (highest impedance), 50 ohm lines (if realizable), and maximum width (lowest impedance) transmission lines. The coupled line characteristics for minimum, nominal, and wide width and spacing include the appropriate coupled transmission line parameters (Z_{even}, Z_{odd}, c, γ_{even}, γ_{odd}, where $\gamma = \alpha + j\beta$).

C. Synthesis Parameter File

A series of parametric subnetworks are predefined and used as templates to realize the desired component specifications. These sub-networks are defined to consume less area than a target (0805) SMT component. Using information from the Technology File and the Electrical Parameter File, analytical models and electromagnetic (EM) simulation tools are used to generate models. For the case of EM tools, further sequential optimization is used on the S-parameter models to obtain equivalent circuit models for better interpolation and extrapolation. At this point we have PSN physical parameters mapped to the electrical R, L, C values. The next step is to reorient this mapping for the Synthesis Parameter File where the primary electrical parameters (R, L, or C) are mapped to various PSN's and their physical parameters (L1, L2, etc) for a specified Technology File (Fig. 2). In many cases there will be more than one possible PSN for a circuit component value. Alternate qualifying attributes will be used to determine which of the PSN's will be utilized.

Fig. 2. Synthesis Parameter File Generation Flow Chart.



III. Model Correlation in Two Material Domains

With Synthesis Files from two material domains and the knowledge of which PSN's have similar parasitics, a variation of space mapping [10] is utilized to identify the parameter mappings between the prototype and production component representations. The library of parts for the prototype phase utilize discrete values (and expected tolerances). Prior to the design phase, these

components need to be manufactured and deployed to the design teams.

IV. Design Phase Utilization

Once the CAD environment is established, design engineers place components onto schematics and specify electrical parameters (impedance, inductance, capacitance, or resistance: Zo, L, C, R) and the details of how this component is realized are automated within the CAD environment. With this improved process, components are represented as parametric sub-networks (PSN) that are interchangeable between specialized SMT (prototype) components or PCB integrated (production) components.

The PSN accesses files that contain data about the reference technology and circuit synthesis (transmission line and integrated passive electrical to physical parameter mappings) are used to generate the layout and simulation models for components based on the physical realization. By changing the technology reference, (and associated files) then generating new synthesis files, the CAD environment can generate layout and simulation models for the specific component value on the new PCB technology without changing schematic components.

For the prototype phase, the Technology File defines SMT parts that use an inverted microvia structure. This allows for rework, tuning, and bench work essential for RF design. For the production phase, these components are transformed into integrated passives using metal etch and the microvia layers in the PCB at no additional per-component cost. Additionally, each integrated passive component is eliminated from the pick and place machine BOM reducing the manufacturing time. By eliminating dozens of components per board in a full production run, engineering costs of this process are quickly recovered.

V. An Example

An initial example of this process is presented in this section. Two compatible material (prodution and prototype) specifications are presented, implications of Electrical Parameter File parameters to the PSN's, a sample list of PSN templates, and an extracted model. The final application of space mapping of models between the two domains is currently in process (current CAD tools don't allow for sufficient automation at this time) but initial assignment of parameter values are quite close.

A. Production Technology

The production material has a 15 mil layer of FR4 and a 2 mil microvia layer. The FR4 material has a nominal value for Er of 4.3, but other FR4 materials and processing can have other Er values (ranging from 3.8 to 4.5) and a loss tangent around 0.018. The microvia layer is often a pure epoxy non-reinforced resin layer (referred to as Resin Coated Copper) with an er of 3.4 and a loss tangent of 0.024.

B. Prototype Technology

Figure 3 shows an example of a discrete valued capacitor on a prototype board. The base FR4 layer is thinner than the production FR4 material layer as a result of the thin layer of air. Solder ball technology is quite important in keeping the amount of solder consistent between repeatable components. Care is also taken to ensure that the bottom plate of the capacitor has the same capacitance to ground in both environments.

With a 1 mil layer of air and solder masking layers strategically placed to reduce the air gaps, the distance from the base plate to the ground plane is reduced from 15 mils in the production material to 12 mils (approximately 11 mils of FR4 and 1 mil of air).

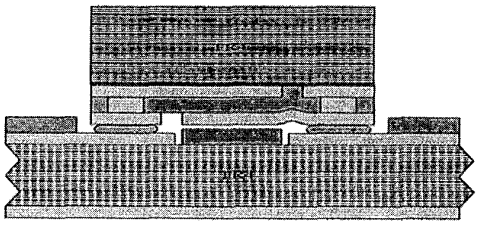


Fig. 3 Prototype Board with FR4 Core Board with mapped SMT discrete valued components.

SMT components are constructed with a thin FR4 board (un-metalized on the top) and microvia layers and solder mask layers on the bottom. The resulting structure mimics the final layer structure of the production component. Care is taken to minimize the air layer thickness and keep the conformal thickness of both sides consistent.

C. Electrical Models

With the base material a different thickness between the two domains, the width of the interconnect lines must be assigned such that their impedance is the same in both domains. If the material specifications of the two domains are properly configured, a line with a specified width should have approximately the same characteristic impedance on the layers defining the component.

D. PSN Templates

Parametric Sub-network templates are very specific to the processing capabilities of a PCB manufacturing facility. As capabilities are enabled, the range of PSN's will be expanded. A summary of some PSN's are presented in Table 1. For resistors, the range of resistivites is quite flexible, resulting in a large domain in which to define specifications.

TABLE 1
SAMPLE PARAMETRIC SUBNETWORK TEMPLATE LISTING

Resistors	Capacitors	Inductors
Straight, Z_{50}	Gap Capacitor	Straight (1), Z_{min}
Straight, Z_{IC}	Inter-digital (2)	Straight (2), Z_{min}
Straight, Z_{min}	Inter-digital (4)	Meander (L), Z_{min}
Meander, Z_{50}	Inter-digital (6)	Meander (W), Z_{min}
Meander, Z_{IC}	Thin Film (uVia)	Spiral (1.5 Turns)
Meander, Z_{min}	TFC - composite	Spiral (2.5 Turns)

E. Synthesis Parameters

Taking a capacitor defined by the two layers on either side of the thin microvia layer, using a 2 mil thick epoxy and a common area between the top and bottom plates of about 30milx30mil and performing a planar 3D EM analysis on the prototype and production stratification, similar models are extracted (Table 2). By sweeping parameters and using space mapping techniques one can see how a companion models can be extracted in two carefully selected material domains. The final synthesis representation for this component would have the physical and parasitic description in both domains tied to the primary component value of capacitance (C_s).

TABLE 2 - FIRST ORDER MODEL FOR 30MIL X 30MIL CAPACITOR IN TWO MATERIAL DOMAINS

	Production	Prototype
C_s	0.430 pF	0.429 pF
L	0.425 nH	0.313 nH
R_{cs}	1.0 ohm	1.6 ohm
R_g	40 kohm	48 kohm

VI. CONCLUSION

By specifying two material stratifications, building and linking companion models (through space mapping across these material domains) a CAD process has been introduced that provides the best aspects of SMT PCB design methodology for the prototype phase and significant benefits for cost reductions while in production. Through this CAD process, integrated passives can be incorporated into PCB designs with minimal risk to already tight production schedules and performance metrics. A wide range of resistor, inductor, and capacitor values are realizable in both material domains. Some components will be more easily realized with standard SMT parts, and others will be more easily realized as integrated passives. The statistical behavior of integrated passive components are clearly defined by material and process variations, resulting in quantified ranges of values for statistical design techniques and greater confidence in production.

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